forming a fill layer on the conductive layer, wherein the fill layer fills the opening, further wherein the fill layer comprises a filler material selected from the group consisting of photoresists and high etch-rate oxides;

removing the conductive layer and the fill layer to a level below a top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer,wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides, and wherein forming the dielectric cap includes:

forming a layer of the at least one dielectric material on the insulating layer, the conductive layer and the fill layer; and

removing the layer of the at least one dielectric material from the insulating layer and the fill layer; and

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.

REMARKS

Claims 117-121 are added; as a result, claims 10-22, and 109-121 are now pending in this application.

§103 Rejection of the Claims

Claims 10, 15, 16, 17, and 20 were rejected under 35 USC §103(a) as being unpatentable by Figura et al. (U.S.6,255,687) in view of Dennison et al.(U.S. 5,888,877) and Chen (U.S. 6,077,743).

Applicant respectfully traverses the rejection. Dennison et al. is not prior art under 35 U.S.C. §103 against any subject matter in the present application that was not present in Dennison et al. The applicable portion of 35 U.S.C. §103 states:

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more subsections (e), (f), and (g) of §102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

35 U.S.C. §103(c) is effective for applications filed on or after November 29, 1999. MPEP §706.02(l)(1) provides further guidance as to the applicability of 35 U.S.C. §103(c) and specifically states:

> Effective November 29, 1999, subject matter which was prior art under former 35 U.S.C. §103 via 35 U.S.C. §102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person." This change to 35 U.S.C. §103(c) applies to all utility, design and plant patent applications filed on or after November 29, 1999, including continuing applications filed under 37 CFR 1.53(b), continued prosecution application filed under 37 CFR 1.53(d), and reissues. The amendment to 35 U.S.C. 103(c) does not affect any application filed before November 29, 1999, a request for examination under 37 CFR 1.129 of such an application, nor a request for continued examination of such an application. The mere filing of a continuing application on or after November 29, 1999 will serve to exclude commonly owned 35 U.S.C. § 102(e) prior art that was applied, or could have been applied, in a rejection under 35 U.S.C. §103 in the parent application.

The present application is a continued patent application filed under 37 C.F.R.1.53(d) on August 30, 2001. This is after the November 29, 1999 effective date of 35 U.S.C. §103(c) as amended in the American Inventors Protection Act of 1999. Accordingly, 35 U.S.C. §103(c), as amended, applies to the present application.

The subject matter of Dennison et al. and the invention defined in the present claims was under an obligation of assignment to the same inventive entity. Applicants point to the following facts as proof of this assertion. First, Dennison et al. is assigned to Micron Technology, Inc. of Boise, ID. as indicated on the face of the patent. Second, the present application is also assigned to Micron Technology, Inc. of Boise, ID. Accordingly, Dennison et al. and the present application are commonly owned.

Accordingly, Applicants respectfully submit that Dennison et al. is disqualified as a prior art reference based at least on the above.

Further, Applicant does not admit that Chen et al. (issued June 20, 2000), Dennison et al. or Figura et al. are prior art and reserves the right to swear behind the documents at a later date. The present application is a continued patent application and the original patent (U.S. 6,303,956) was filed February 26, 1999.

Applicant also believes that Figura et al. (U.S. 6,225,687) is not prior art under 35 U.S.C. §103 as Figura et al. has a filing date (September 29, 1999) after the filing date of the present application and both Figura et al. and the present application are assigned to Micron Technology Inc.

Applicant requests reconsideration and allowance of claims 10, 15, 16, 17, and 20.

Claims 18, 19, 22, and 109-116 were rejected under 35 USC §103(a) as being unpatentable over Figura et al. (U.S. 6,255,687) as applied to claims 10 and 20 above, and further in view of Abernathey et al. (U.S. 4,725,560).

Claims 18 and 19 are dependent on claim 10, and claim 22 is dependent on claim 20. The rejection applies Figura to 18, 19, 22 and 109-116 as applied to claims 10 and 20. Thus, although the rejection only mentions Figura, it appears the Office Action is relying on the proposed combination of Figura, Dennison, and Chen mentioned previously with a further proposed addition of Abernathey. Applicant therefore respectfully traverses the rejection for the reasons stated previously and requests reconsideration and allowance of claims 18, 19, 22, and 109-116.

Allowable Subject Matter

Claims 11-14 and 21 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant believes these claims are allowable with their respective parent claims and does not rewrite these claims at this time.

New Claims

New claim 117 recites language essentially found in unamended claims 10 and 11. New claims 117-120 generally correspond to claims 11-14. New claim 121 recites language essentially found in unamended claims 20 and 21. Consideration of new claims 117-121 is requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6904) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

GURTEJ SINGH SANDHU ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 31 Jan 2003 By _____
Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 31st day of January, 2003.

Name Amy Moriarty Signature _____

Docket No. 303.541US2
WD # 473054

Micron Ref. No. 98-0607.01

Clean Version of Pending Claims

CONDUCTIVE CONTAINER STRUCTURES HAVING A DIELECTRIC CAP
Applicant: Gurtej Singh Sandhu et al.
Serial No.: 09/945,397

Claims 10-22 and 109-121, as of January 31, 2003 (date response to first office action filed).

10. A method of forming a semiconductor structure, comprising:

forming an insulating layer on a substrate;

forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening;

removing the conductive layer and the fill layer to a level below a top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer;

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.

11. The method of claim 10, wherein the processing proceeds in the order presented.

12. The method of claim 10, wherein removing at least a portion of the insulating layer to expose an outside of the container structure occurs subsequent to forming a dielectric cap on a top of the sidewalls of the conductive layer.

13. The method of claim 10, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:

forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and

removing the dielectric layer from the insulating layer and the fill layer.

14. The method of claim 13, wherein removing the dielectric layer from the insulating layer and the fill layer further comprises removing the dielectric layer from the insulating layer and the fill layer using an anisotropic etch.

15. The method of claim 10, wherein forming an insulating layer on a substrate further comprises forming a layer of borophosphosilicate glass on the substrate.

16. The method of claim 10, wherein forming a conductive layer on the insulating layer and the exposed portion of the substrate further comprises forming a layer of conductively-doped hemispherical grain polysilicon on the insulating layer and the exposed portion of the substrate.

17. The method of claim 10, wherein forming a fill layer on the conductive layer further comprises forming a layer of photoresist on the conductive layer.

18. The method of claim 10, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises forming a cap of silicon oxynitride on a top of the sidewalls of the conductive layer.

19. The method of claim 10, further comprising:
annealing the dielectric cap.

20. A method of forming a semiconductor structure, comprising:

forming an insulating layer on a substrate, wherein the insulating layer comprises at least one insulating material selected from the group consisting of oxides, nitrides and borophosphosilicate glass;

forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate, wherein the conductive layer comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening, further wherein the fill layer comprises a filler material selected from the group consisting of photoresists and high etch-rate oxides;

removing the conductive layer and the fill layer to a level below a top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides;

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.

21. The method of claim 20, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:

forming a layer of the at least one dielectric material on the insulating layer, the

conductive layer and the fill layer; and

removing the layer of the at least one dielectric material from the insulating layer and the fill layer.

22. The method of claim 20, further comprising:

annealing the dielectric cap.

109. A method of forming a semiconductor structure, comprising:

forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom; and

forming a dielectric cap on a top of the sidewalls.

110. The method of claim 109, wherein the processing proceeds in the order presented.

111. The method of claim 109, wherein forming a dielectric cap on a top of the sidewalls further comprises forming a dielectric cap of silicon oxynitride on a top of the sidewalls.

112. The method of claim 109, further comprising:

annealing the dielectric cap.

113. A method of forming a semiconductor structure, comprising:

forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the conductive container structure comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon; and

forming a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides.

114. The method of claim 113, wherein the processing proceeds in the order presented.

115. A method of forming a semiconductor structure, comprising:
forming a conductive container structure having a closed bottom and sidewalls extending upward from the closed bottom, wherein the conductive container structure comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;
forming a dielectric cap on a top of the sidewalls, wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides; and
annealing the dielectric cap.

116. The method of claim 115, wherein the processing proceeds in the order presented.

117. (New) A method of forming a semiconductor structure, comprising the following processing steps in the order presented:
forming an insulating layer on a substrate;
forming an opening in the insulating layer, wherein the opening has a bottom on an exposed portion of the substrate and sidewalls defined by the insulating layer;
forming a conductive layer on the insulating layer and the exposed portion of the substrate;
forming a fill layer on the conductive layer, wherein the fill layer fills the opening;
removing the conductive layer and the fill layer to a level below a top of the insulating

layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer;

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.

118. (New) The method of claim 117, wherein removing at least a portion of the insulating layer to expose an outside of the container structure occurs subsequent to forming a dielectric cap on a top of the sidewalls of the conductive layer.

119. (New) The method of claim 117, wherein forming a dielectric cap on a top of the sidewalls of the conductive layer further comprises:

forming a dielectric layer on the insulating layer, the conductive layer and the fill layer; and

removing the dielectric layer from the insulating layer and the fill layer.

120. (New) The method of claim 117, wherein removing the dielectric layer from the insulating layer and the fill layer further comprises removing the dielectric layer from the insulating layer and the fill layer using an anisotropic etch.

121. (New) A method of forming a semiconductor structure, comprising:

forming an insulating layer on a substrate, wherein the insulating layer comprises at least one insulating material selected from the group consisting of oxides, nitrides and borophosphosilicate glass;

forming an opening in the insulating layer, wherein the opening has a bottom on an

exposed portion of the substrate and sidewalls defined by the insulating layer;

forming a conductive layer on the insulating layer and the exposed portion of the substrate, wherein the conductive layer comprises at least one silicon material selected from the group consisting of amorphous silicon, polysilicon and hemispherical grain polysilicon;

forming a fill layer on the conductive layer, wherein the fill layer fills the opening, further wherein the fill layer comprises a filler material selected from the group consisting of photoresists and high etch-rate oxides;

removing the conductive layer and the fill layer to a level below a top of the insulating layer, thereby forming a container structure having sidewalls comprised of the conductive layer on the sidewalls of the opening, and a closed bottom comprised of the conductive layer on the bottom of the opening;

forming a dielectric cap on a top of the sidewalls of the conductive layer,wherein the dielectric cap comprises at least one dielectric material selected from the group consisting of oxides, nitrides and silicon oxynitrides, and wherein forming the dielectric cap includes:

forming a layer of the at least one dielectric material on the insulating layer, the conductive layer and the fill layer; and

removing the layer of the at least one dielectric material from the insulating layer and the fill layer; and

removing the fill layer to expose an inside of the container structure; and

removing at least a portion of the insulating layer to expose an outside of the container structure.